FIG. 1

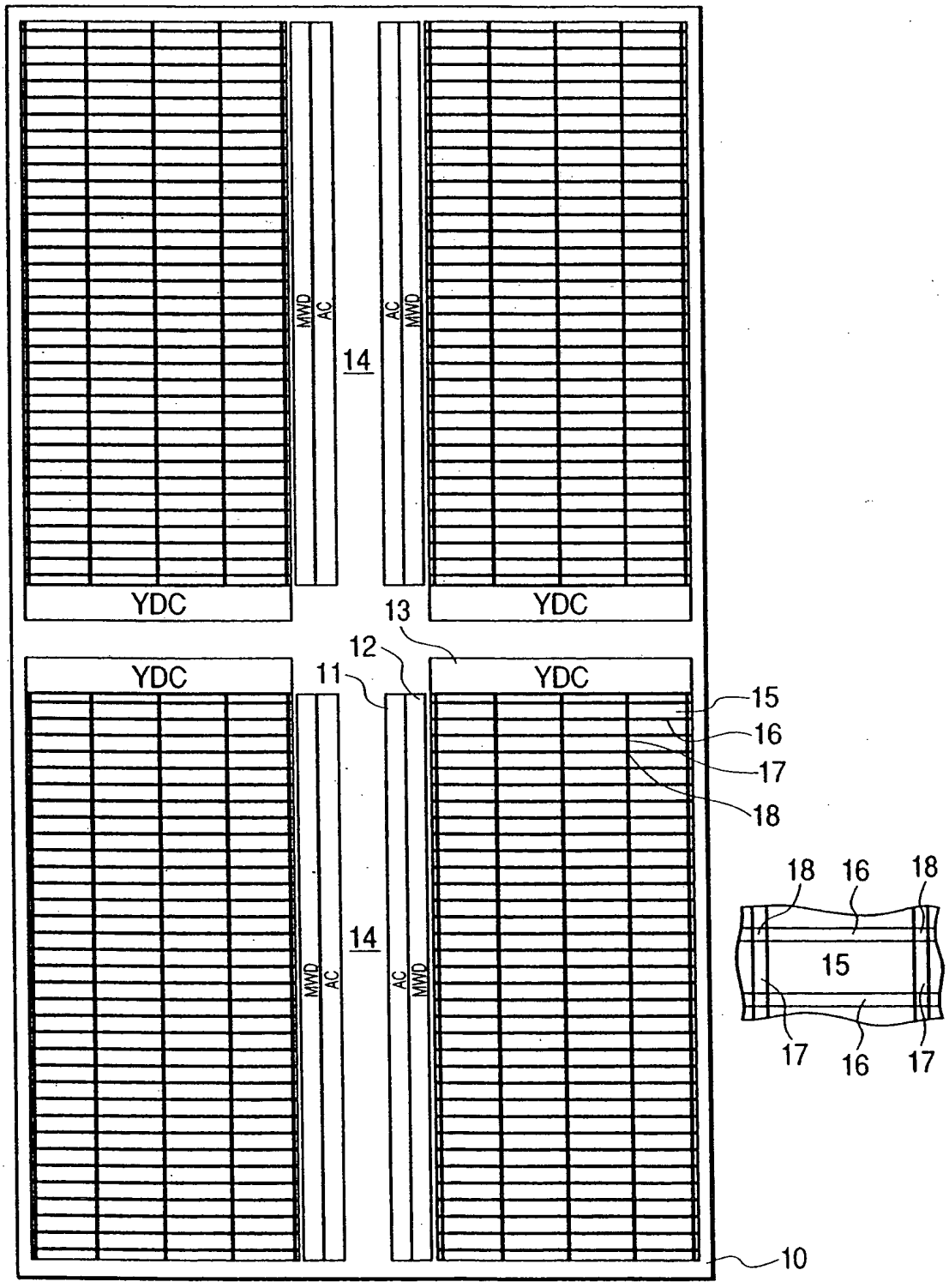

YDC
YDC
YDC
YDC
MWD
AC
AC
MWD
MWD
AC
AC
MWD
14
14
13
12
11
15
16
17
18
18
16
18
15
17
16
17
10

FIG. 2A

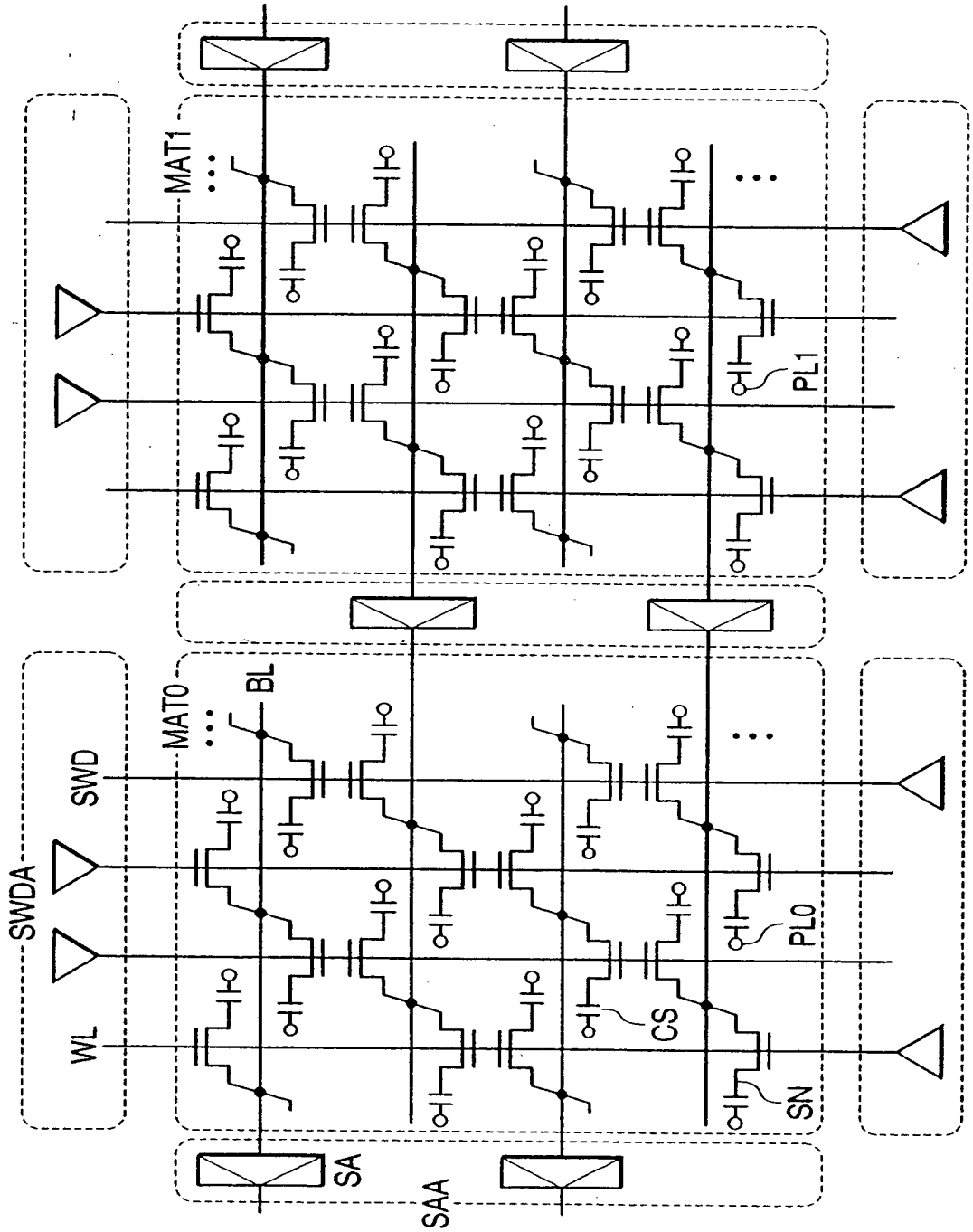


FIG. 2B

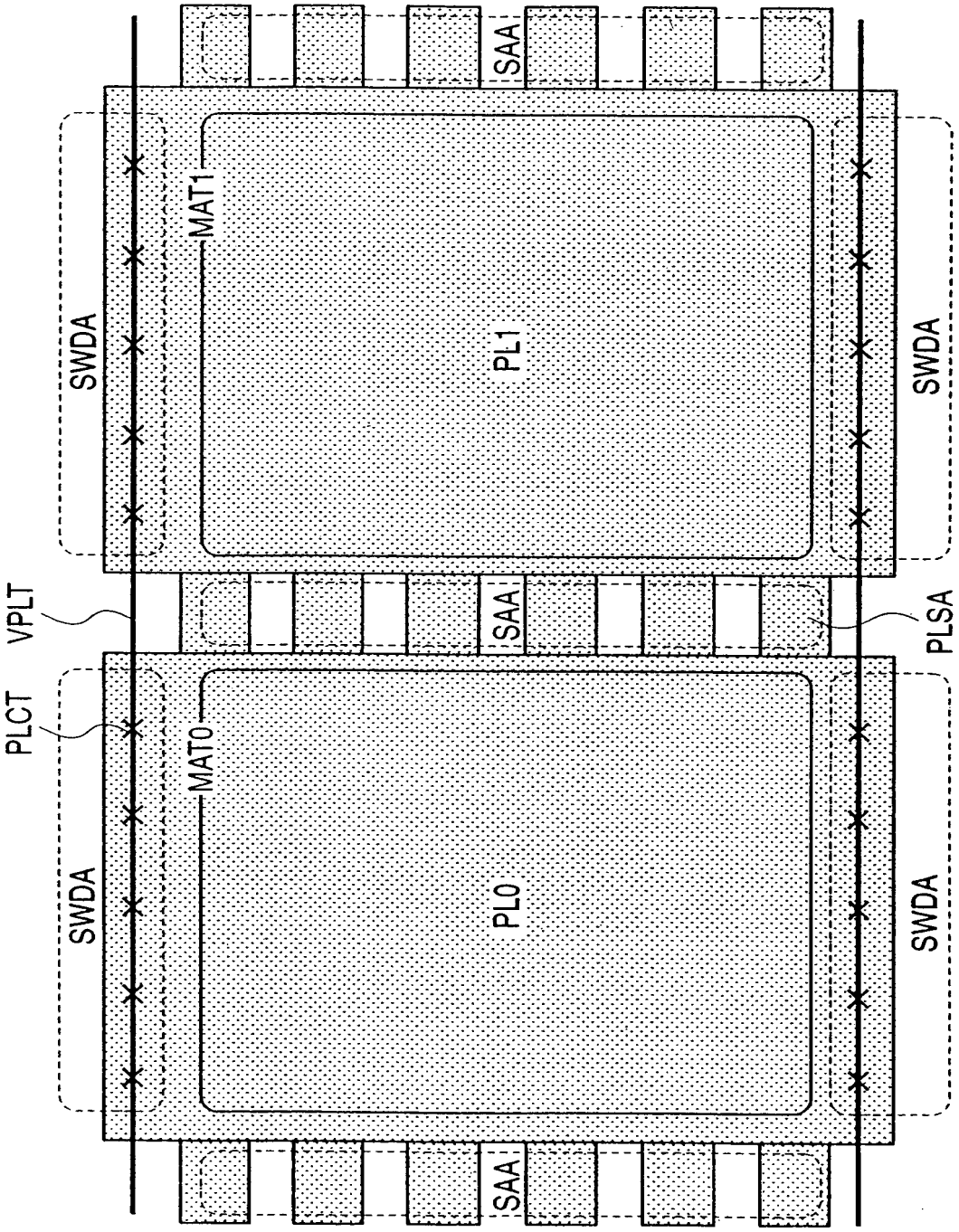

SAA
MAT1
SWDA
PL1
SWDA
VPLT
SAA
PLSA
PLCT
MAT0
SWDA
PL0
SWDA
SAA

FIG. 3A

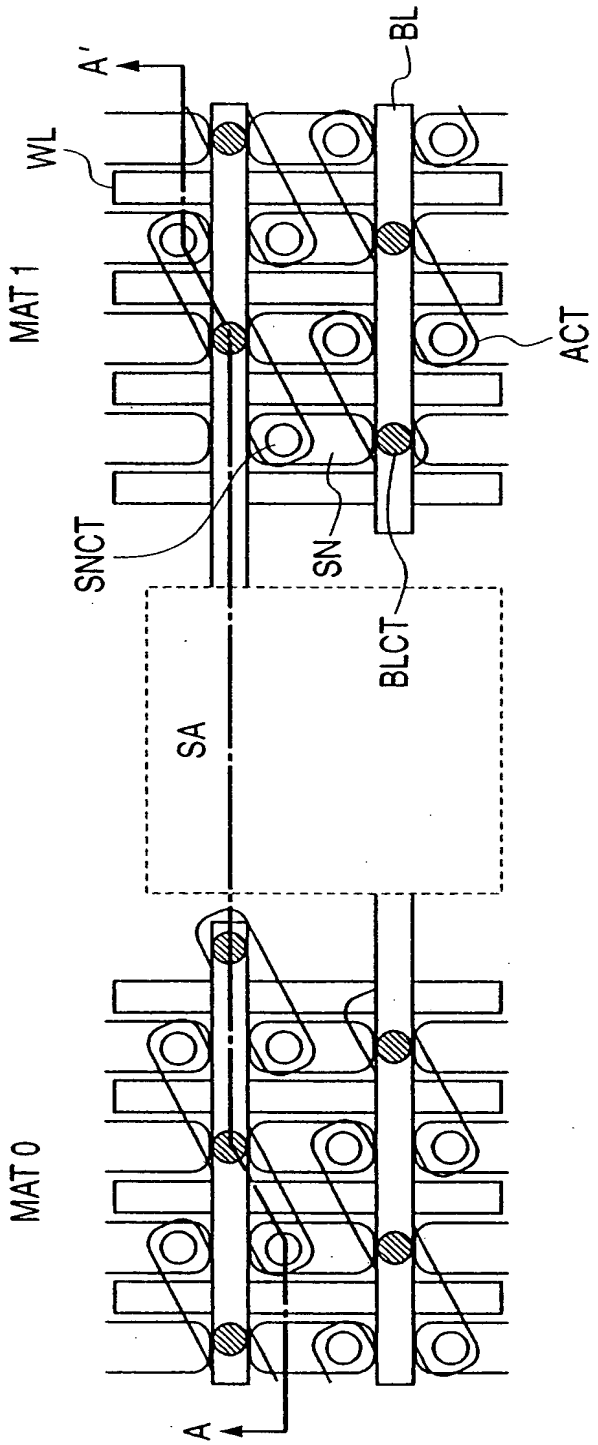


FIG. 3B

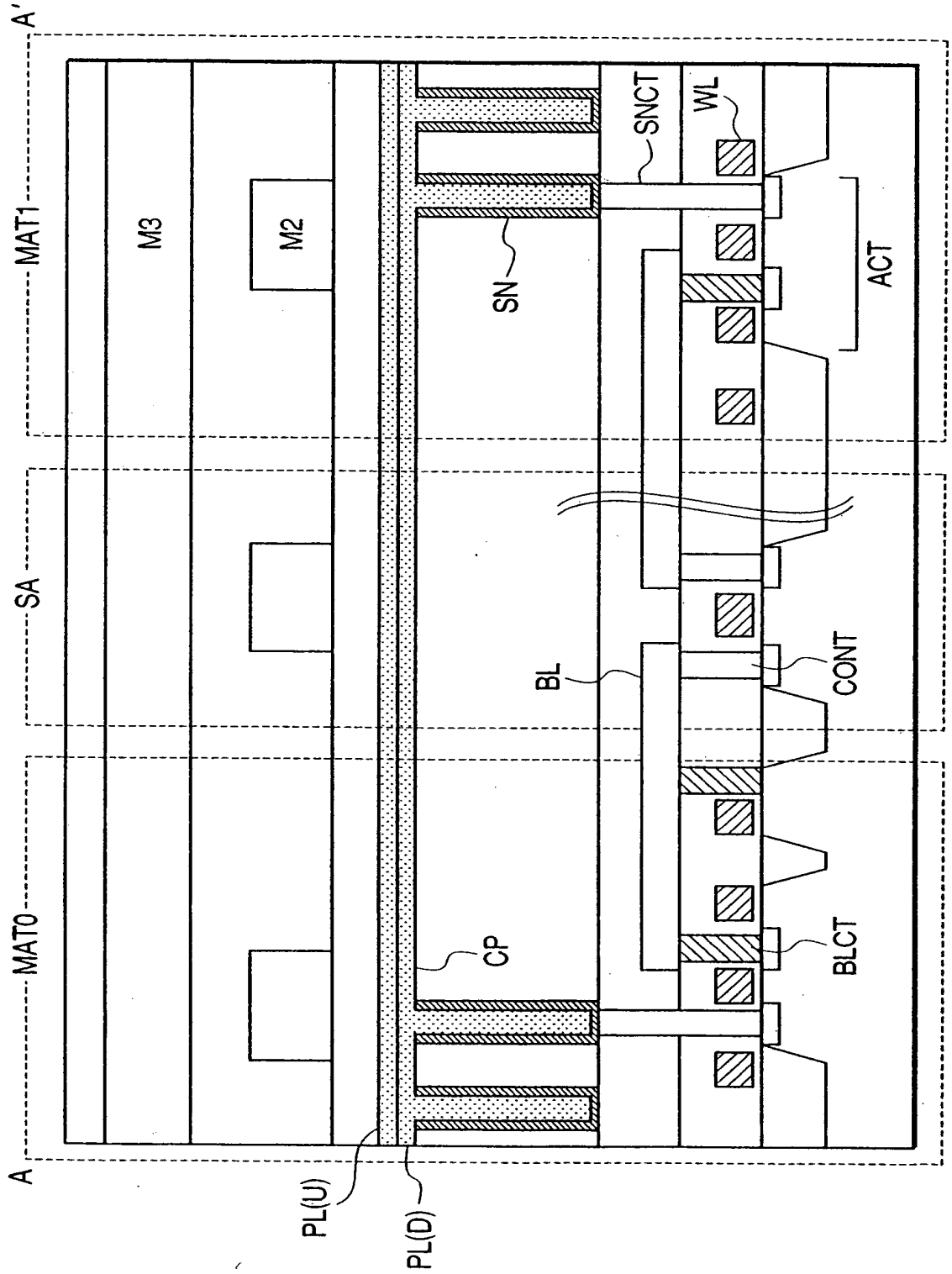


FIG. 4A

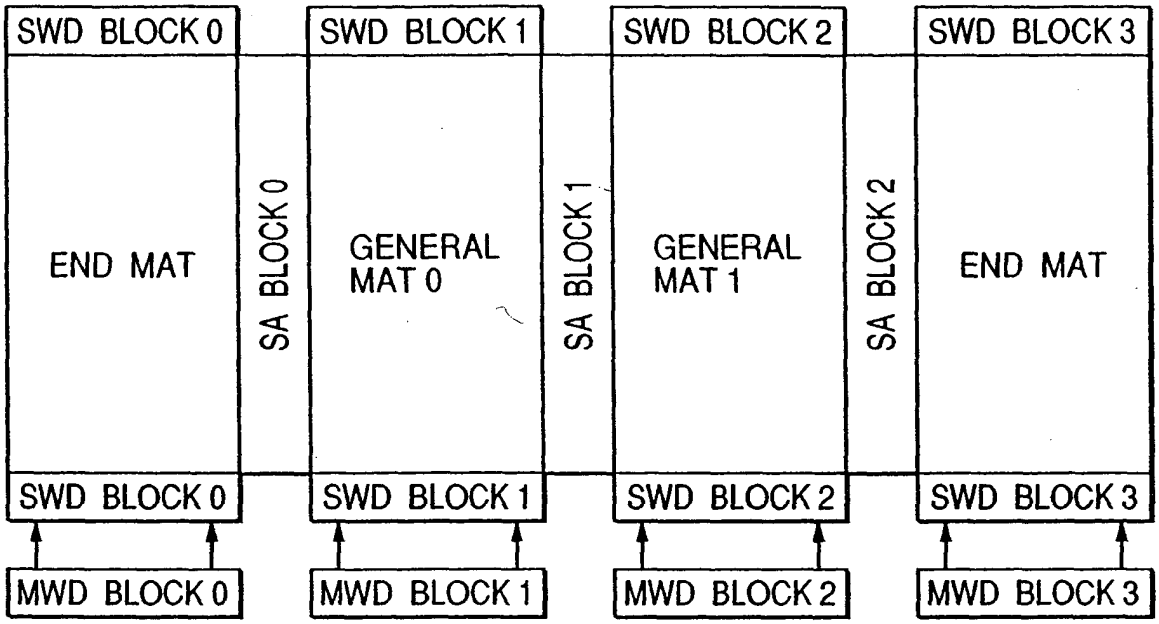


FIG. 4B

IN ACCESSING GENERAL MAT 0 :
SWD BLOCK 1 : ACTIVATED
SA BLOCKS 0,1 : ACTIVATED

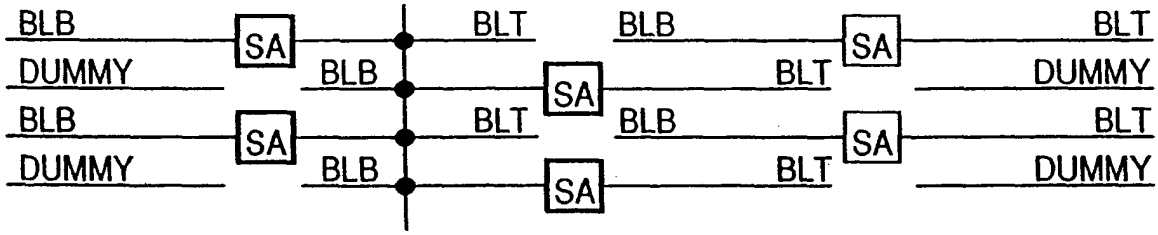


FIG. 4C

IN ACCESSING END MAT :
SWD BLOCKS 0,3 : CONCURRENTLY ACTIVATED
SA BLOCKS 0,2 : ACTIVATED

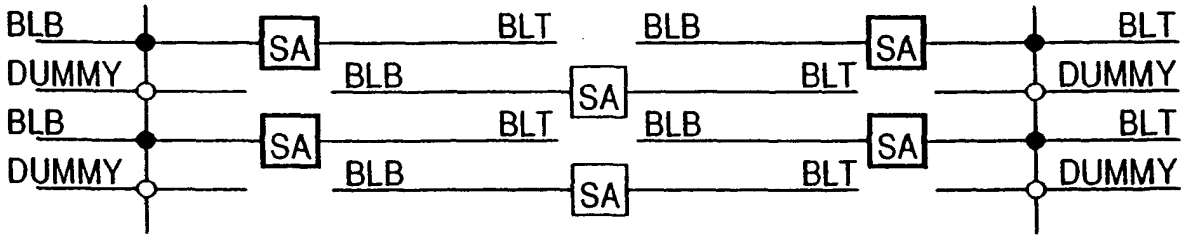


FIG. 5A

GENERAL MAT MWD CIRCUIT EXAMPLE

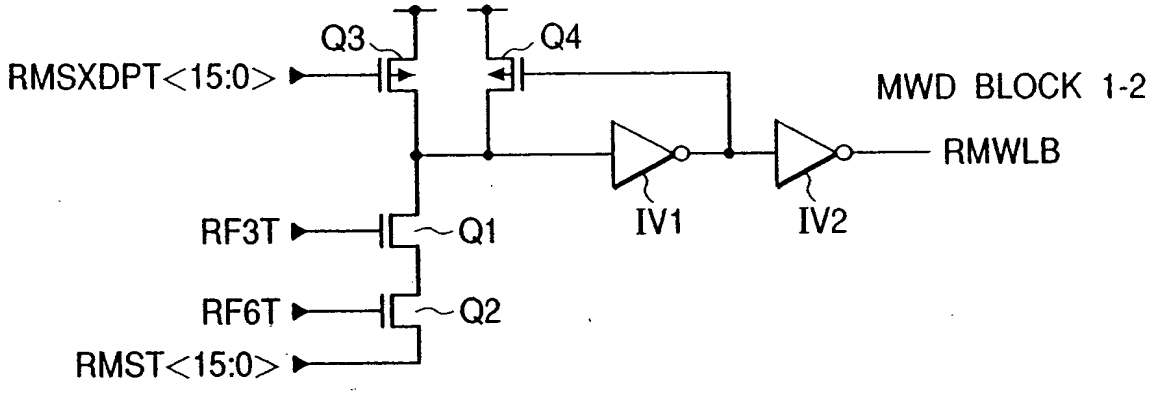
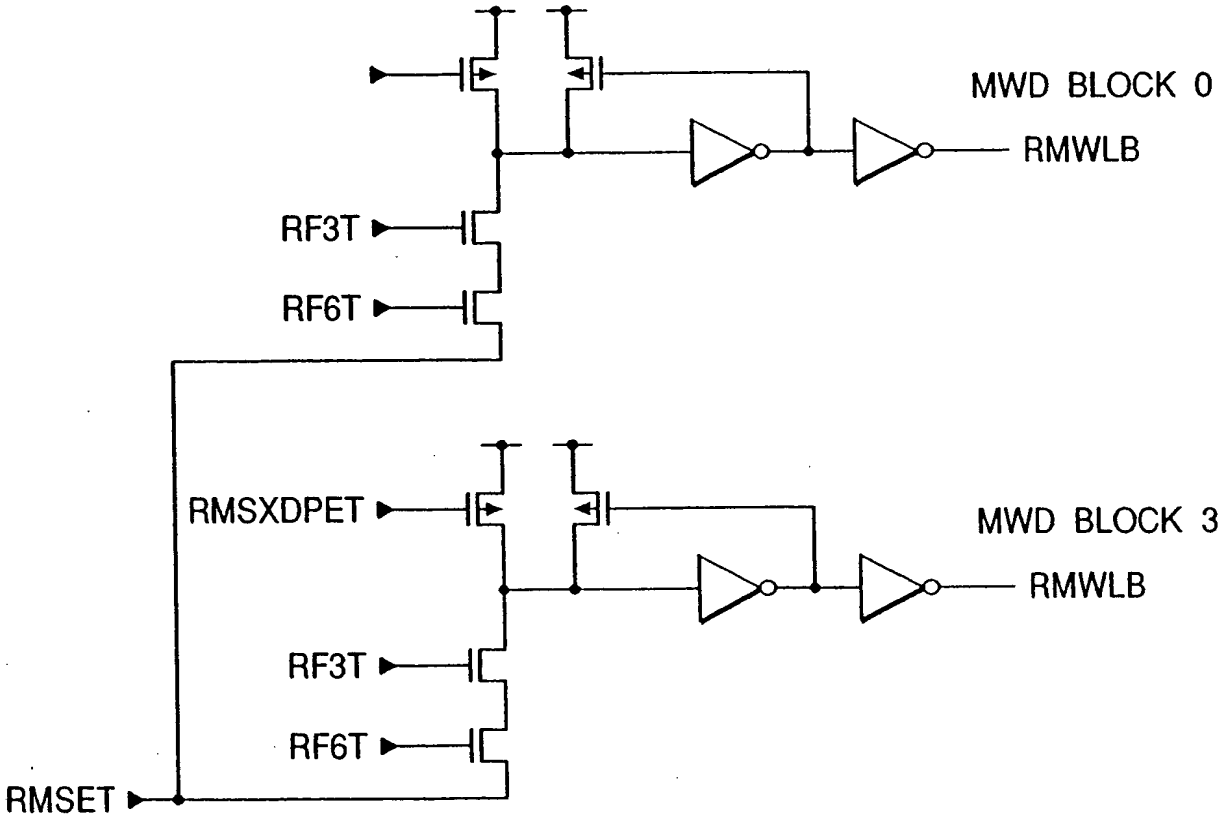


FIG. 5B

END MAT MWD CIRCUIT EXAMPLE



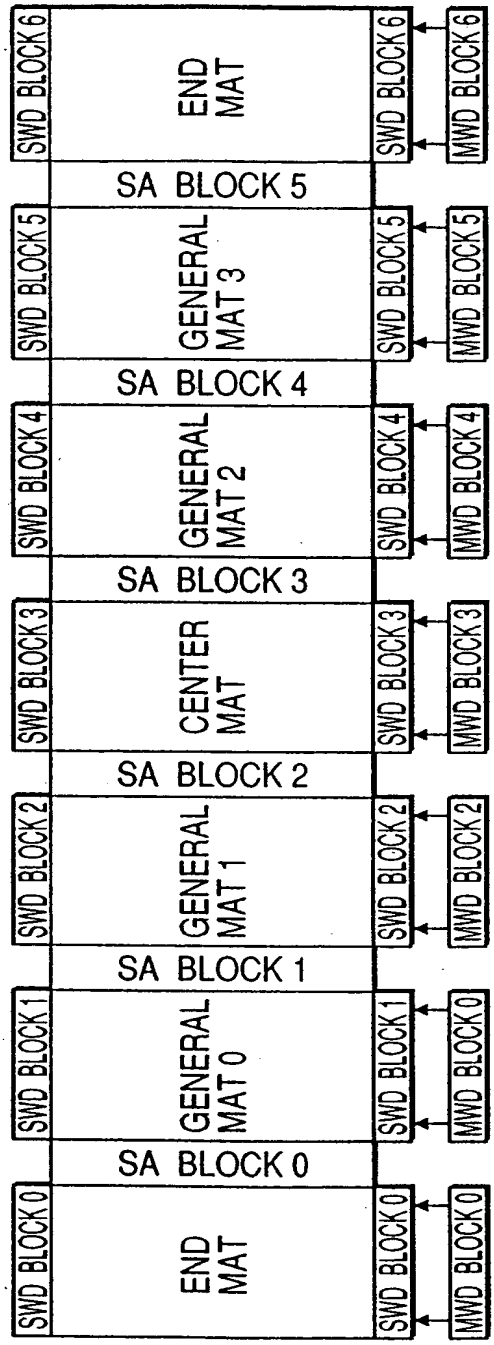


FIG. 6A

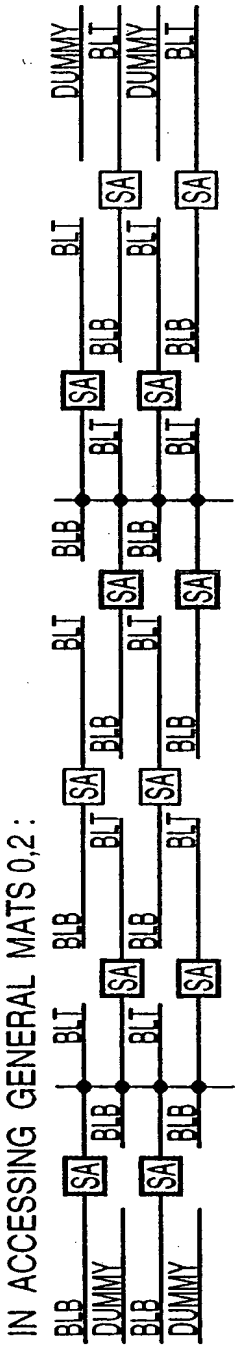


FIG. 6B

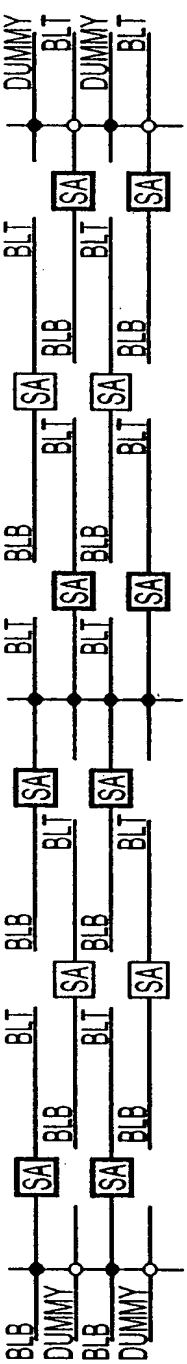
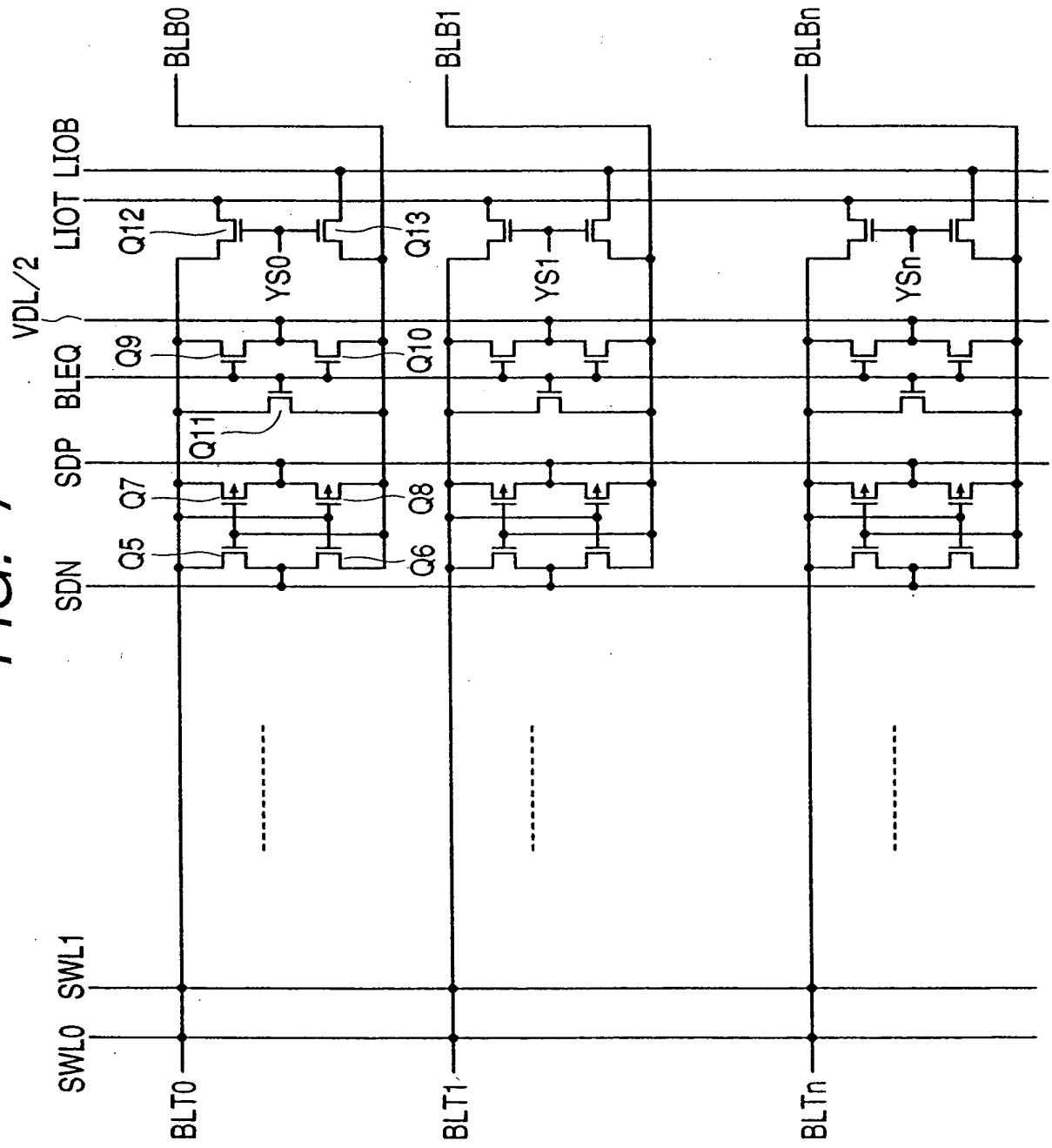


FIG. 6C

FIG. 7


BLB0
BLB1
BLBn
LIOB
LIOT
VDL/2
BLEQ
SDP
SDN
SWL1
SWL0
Q12
Q13
YS0
YS1
YSn
Q9
Q10
Q11
Q7
Q8
Q5
Q6
BLT0
BLT1
BLTn

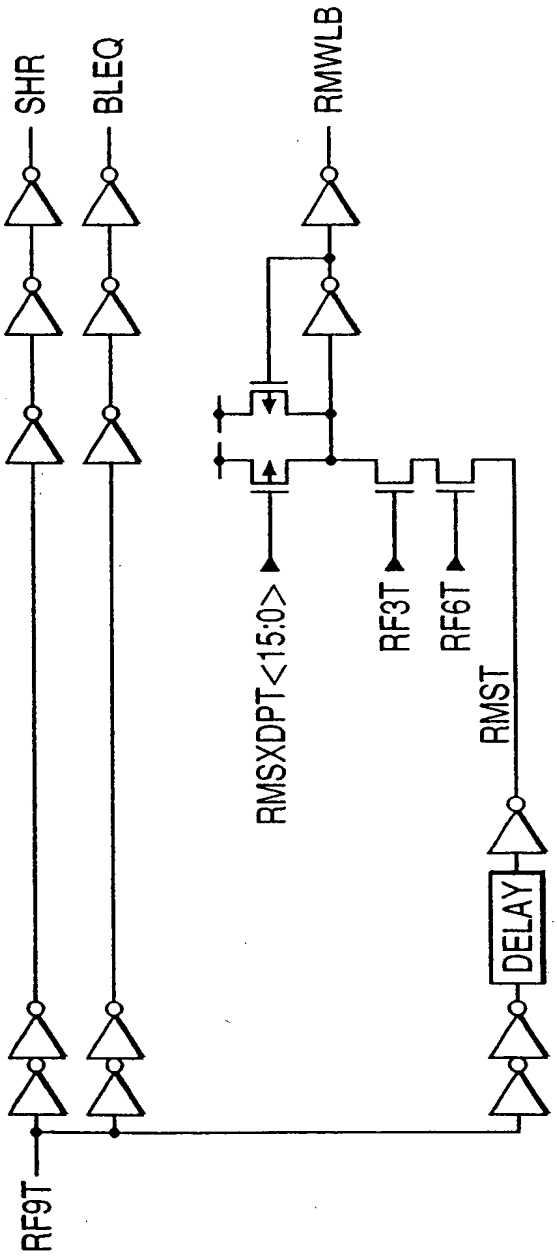

SHR
BLEQ
RMWLB
RMSXDPT<15:0>
RF3T
RF6T
RMST
DELAY
RF9T

FIG. 8A

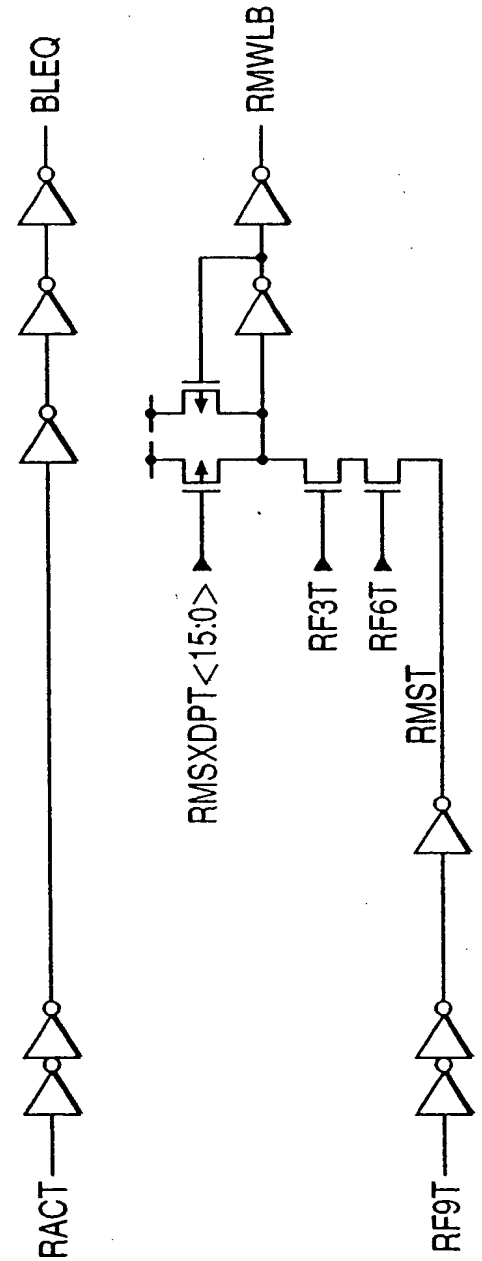

BLEQ
RMWLB
RMSXDPT<15:0>
RF3T
RF6T
RMST
RACT
RF9T

FIG. 8B

FIG. 9A

DELAYS FOR ALLOCATING BLEQ/
SHR⇔SWL TIMING MARGIN ARE REQUIRED :

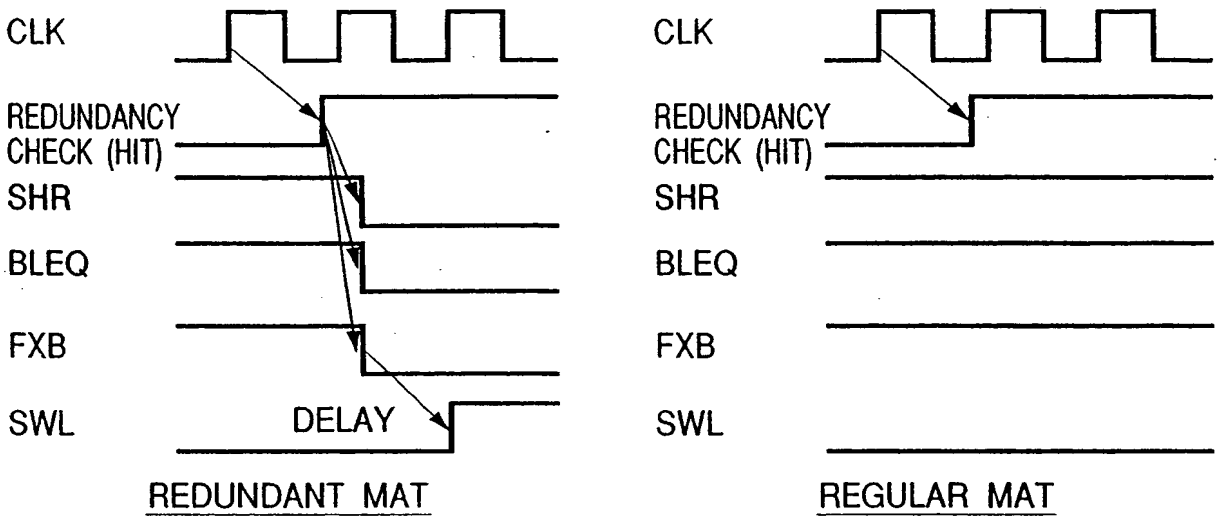


FIG. 9B

NO DELAYS FOR ALLOCATING BLEQ⇔SWL TIMING
MARGIN ARE REQUIRED :

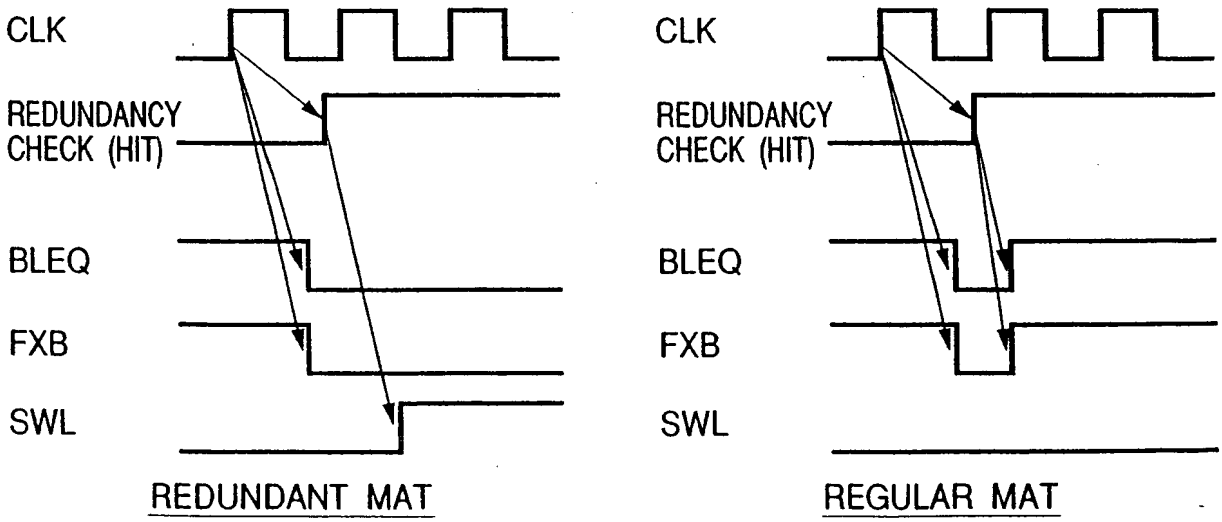
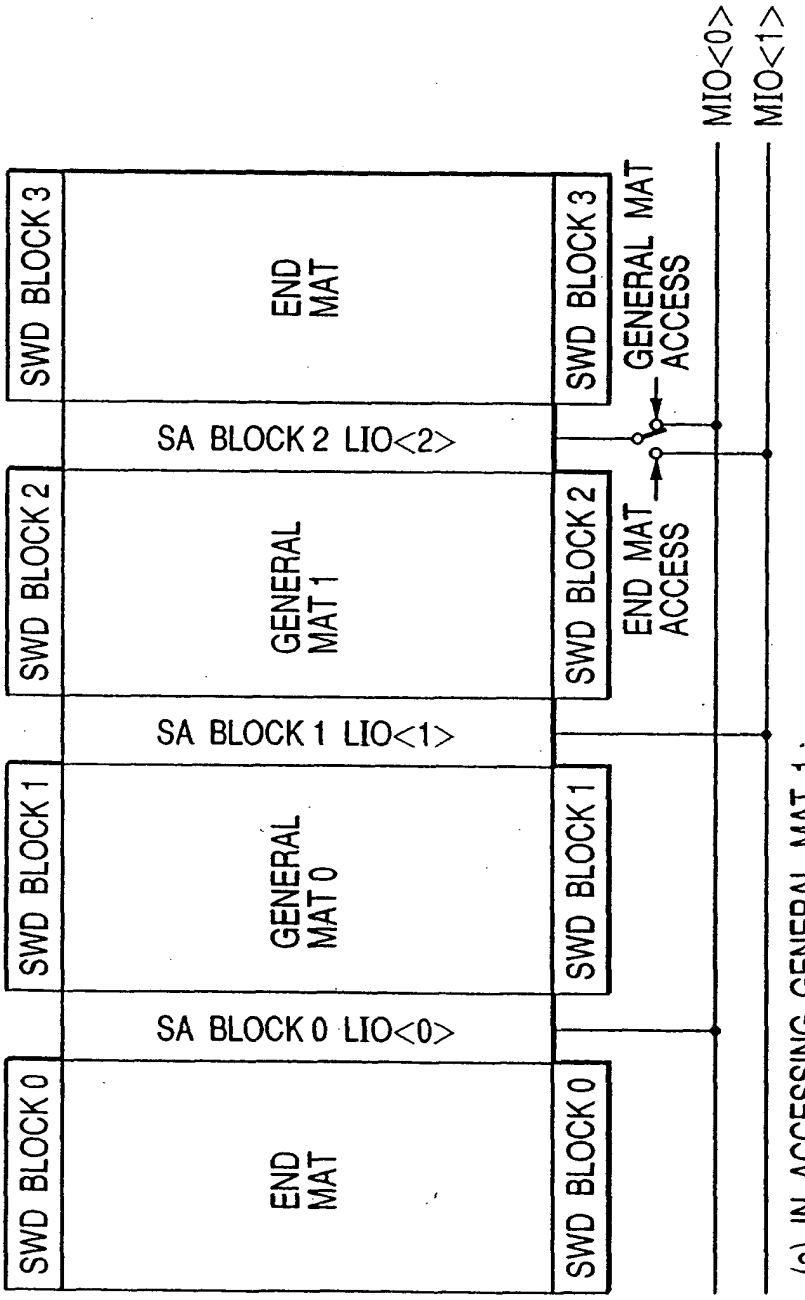


FIG. 10



(a) IN ACCESSING GENERAL MAT 1 :
DATA OUTPUT FROM LIO<1> TO MIO<1>
DATA OUTPUT FROM LIO<2> TO MIO<0>

(b) IN ACCESSING END MAT :
DATA OUTPUT FROM LIO<0> TO MIO<0>
DATA OUTPUT FROM LIO<2> TO MIO<1>

FIG. 11A

GENERAL MATS ON BOTH SIDES

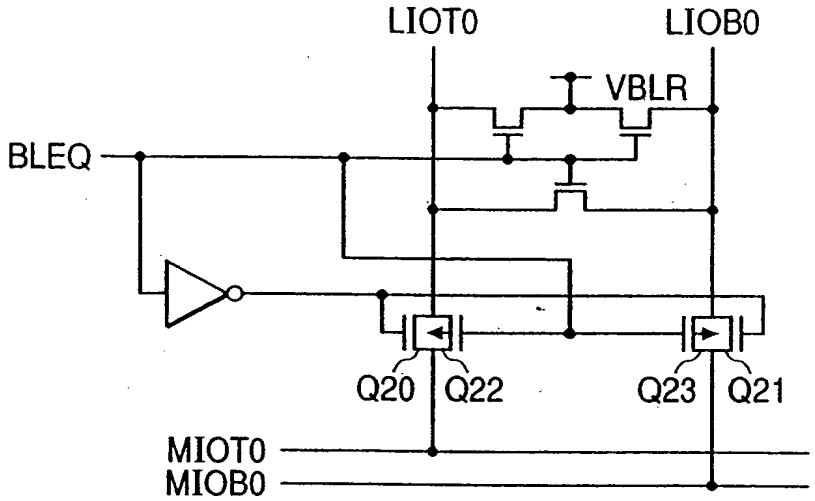


FIG. 11B

END MAT ON ONE SIDE

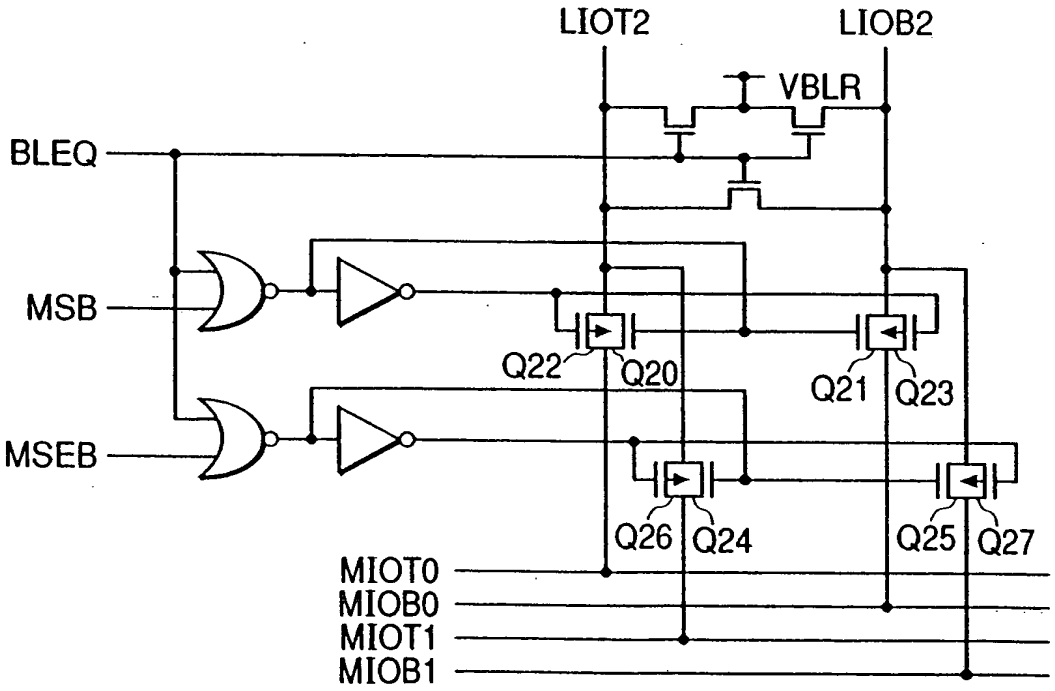
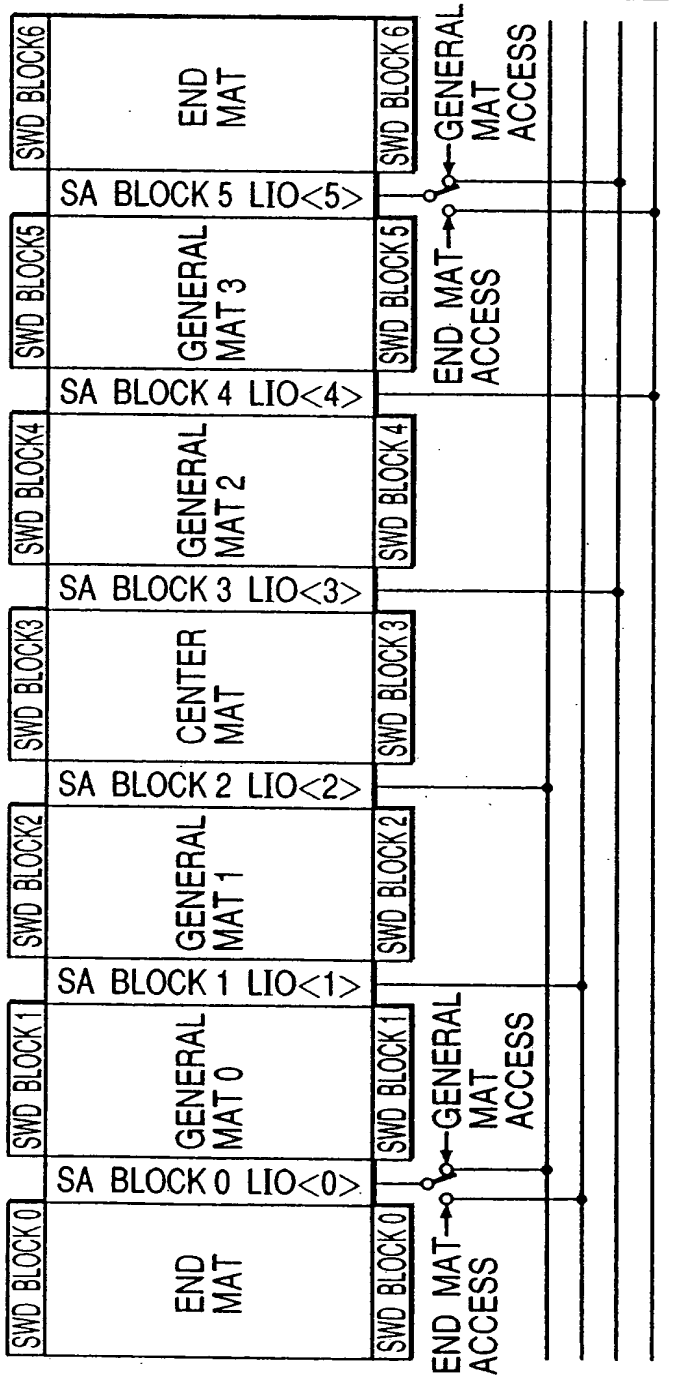


FIG. 12



(a) IN ACCESSING GENERAL MATS 0,2:
CONNECT LIO<0> AND MIO<0>, LIO<1> AND MIO<1>, LIO<3> AND MIO<2>,
AND LIO<4> AND MIO<3>, RESPECTIVELY

(b) IN ACCESSING END AND CENTER MATS:
CONNECT LIO<0> AND MIO<1>, LIO<2> AND MIO<0>, LIO<3> AND MIO<2>,
AND LIO<5> AND MIO<3>, RESPECTIVELY

FIG. 13A

SIMPLE 1 CROSS POINT SENSE AMPLIFIER ALTERNATELY ARRANGED ARRAY

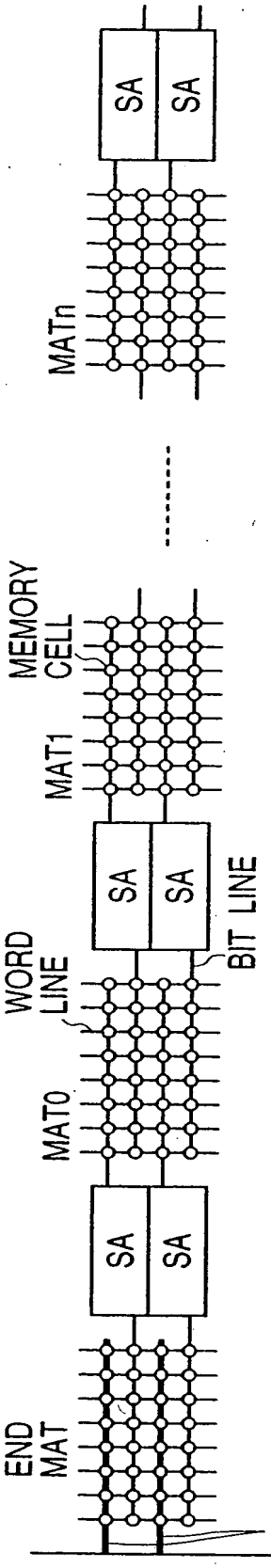


FIG. 13B

PROPOSED FOLDED TYPE ARRAY

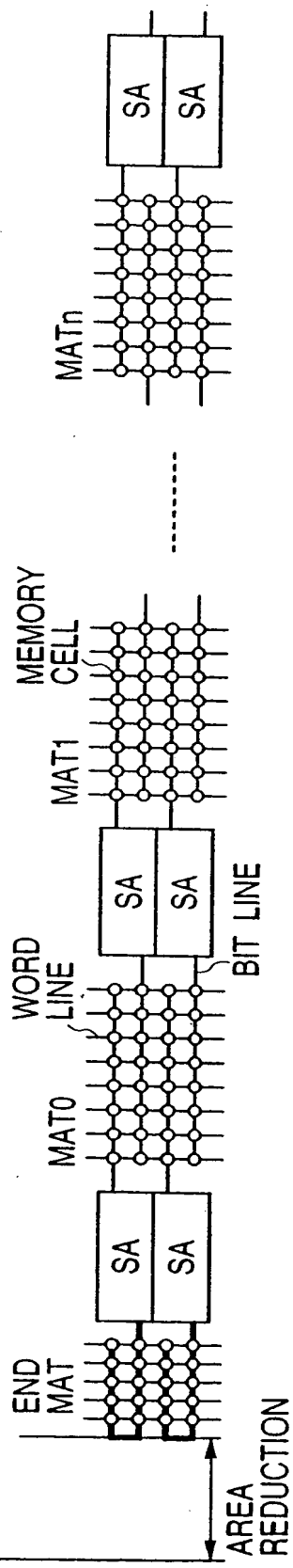


FIG. 14A

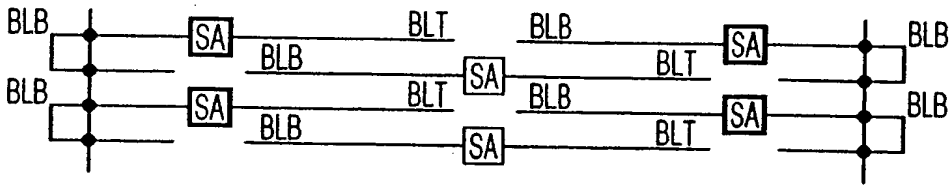


FIG. 14B

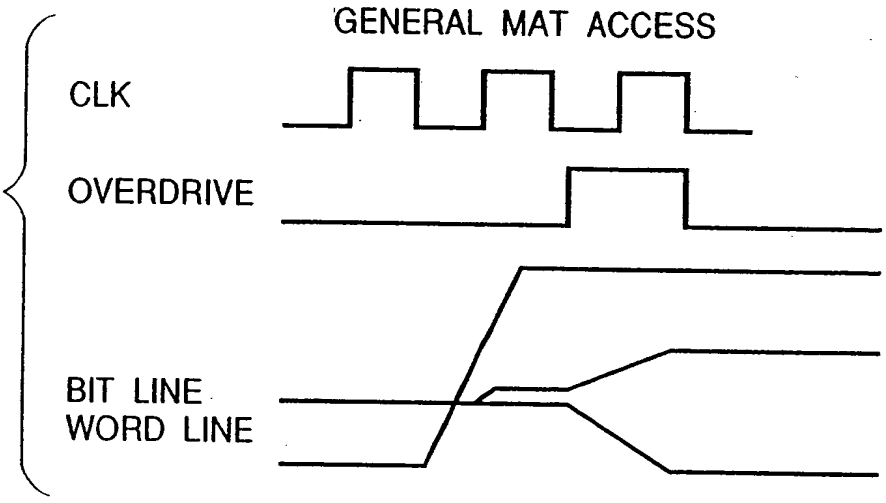


FIG. 14C

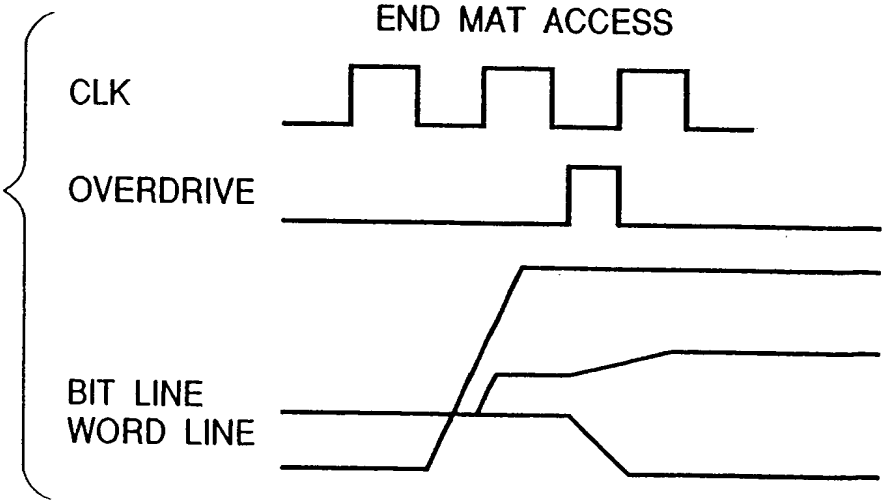


FIG. 15

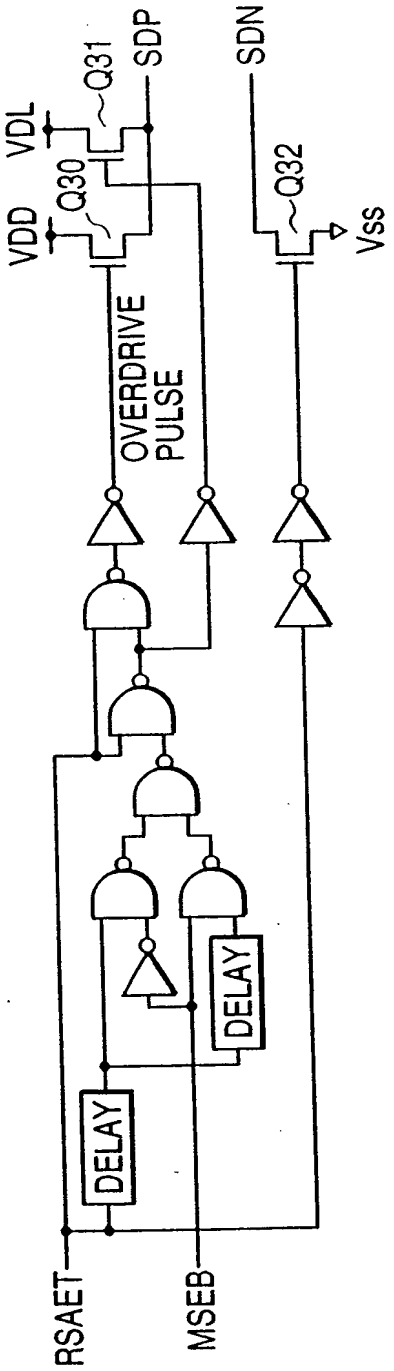

VDL
Q31
SDP
SDN
VDD
Q30
Q32
Vss
OVERDRIVE
PULSE
DELAY
DELAY
RSAET
MSEB

FIG. 16A

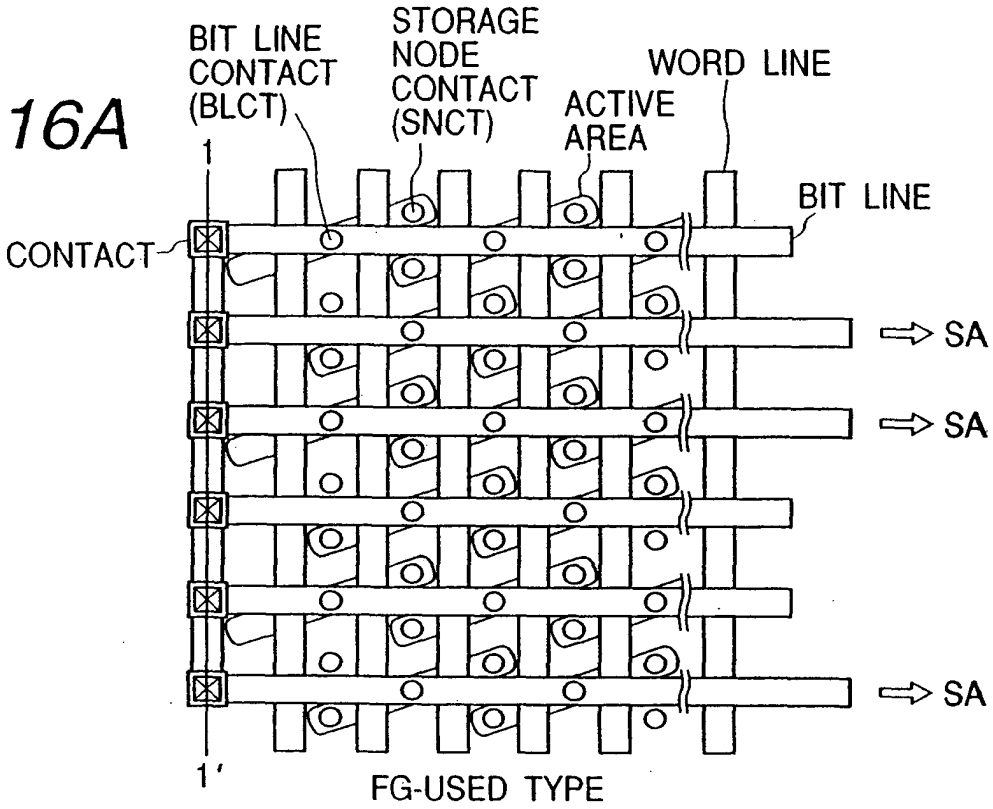


FIG. 16B

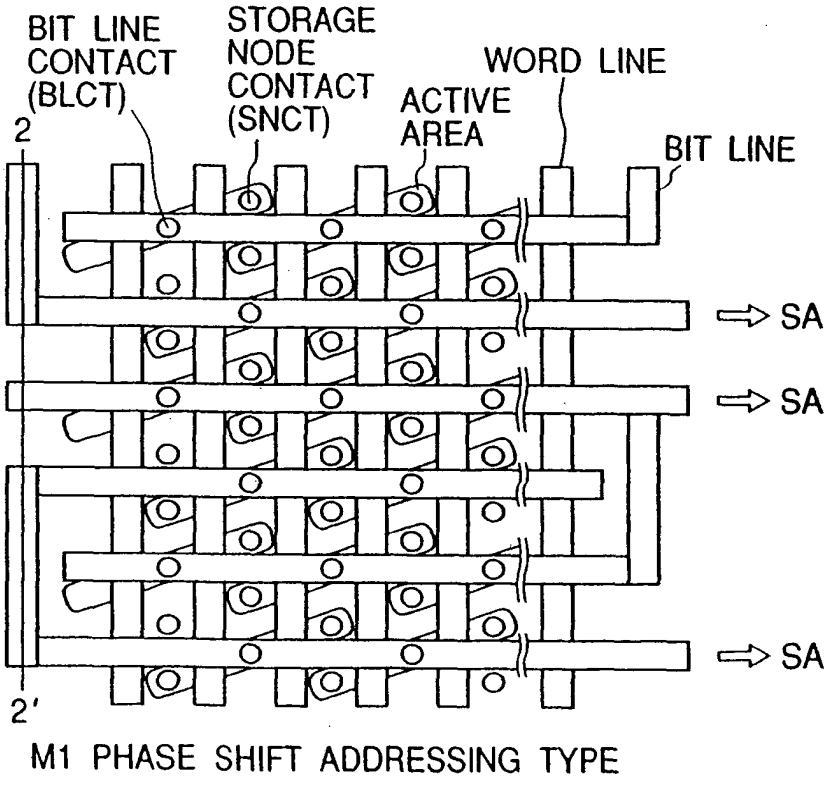
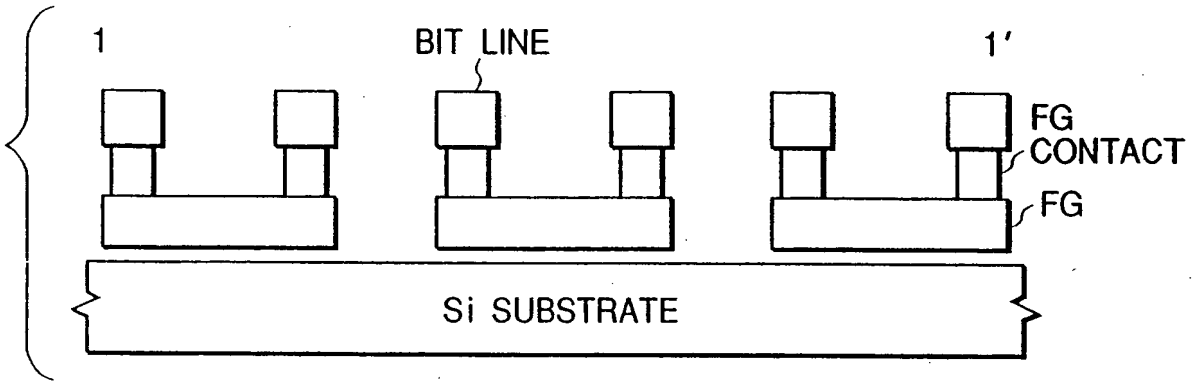
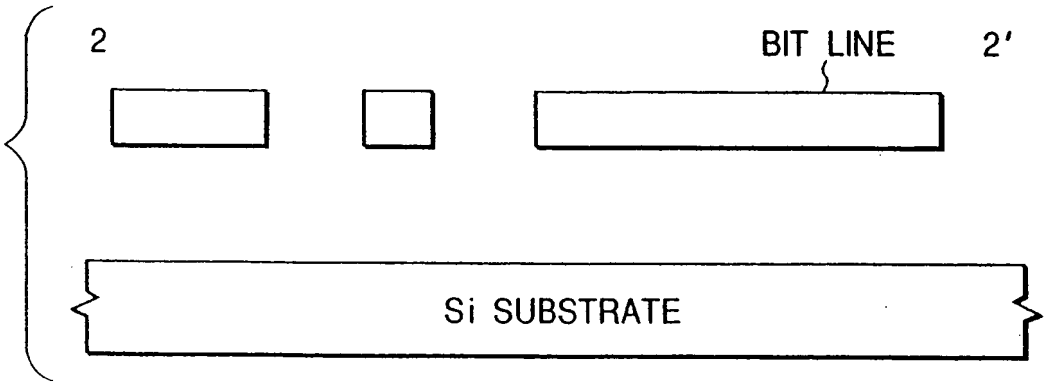


FIG. 17A



CROSS-SECTION 1—1'

FIG. 17B



CROSS-SECTION 2—2'

FIG. 18

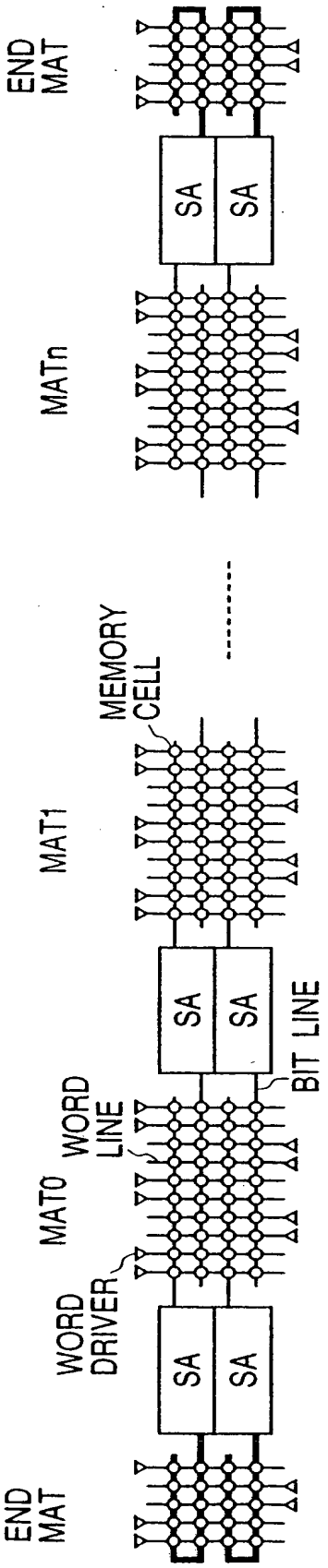

END MAT
MATn
SA
SA
MAT1
MEMORY CELL
MAT0
WORD LINE
BIT LINE
WORD DRIVER
SA
SA
END MAT
VSS OR VDL/2
VSS OR VDL/2

FIG. 19

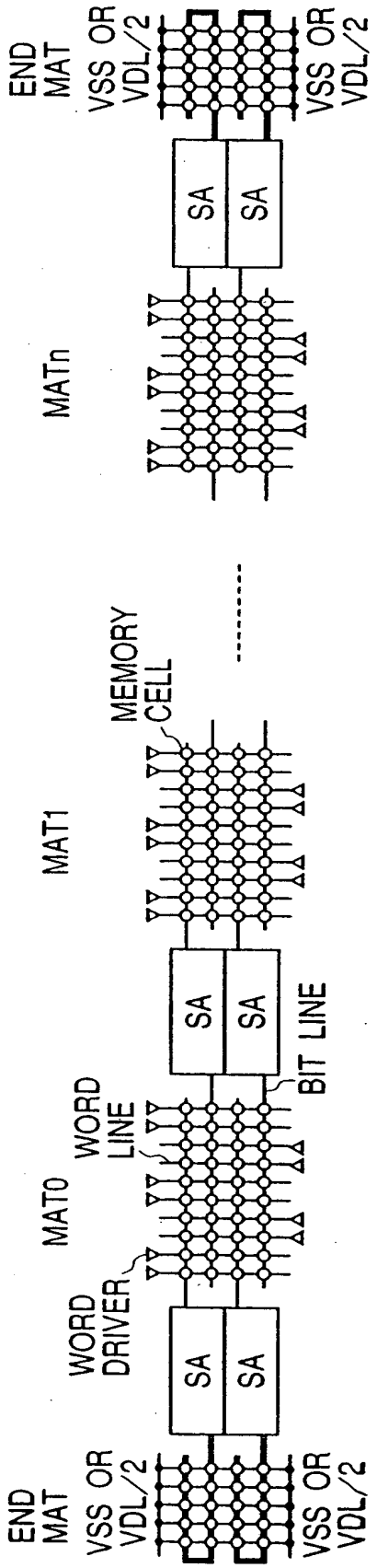

END MAT
VSS OR VDL/2
VSS OR VDL/2
MATn
SA
SA
MAT1
MEMORY CELL
MAT0
WORD LINE
BIT LINE
WORD DRIVER
SA
SA
END MAT
VSS OR VDL/2
VSS OR VDL/2

FIG. 20

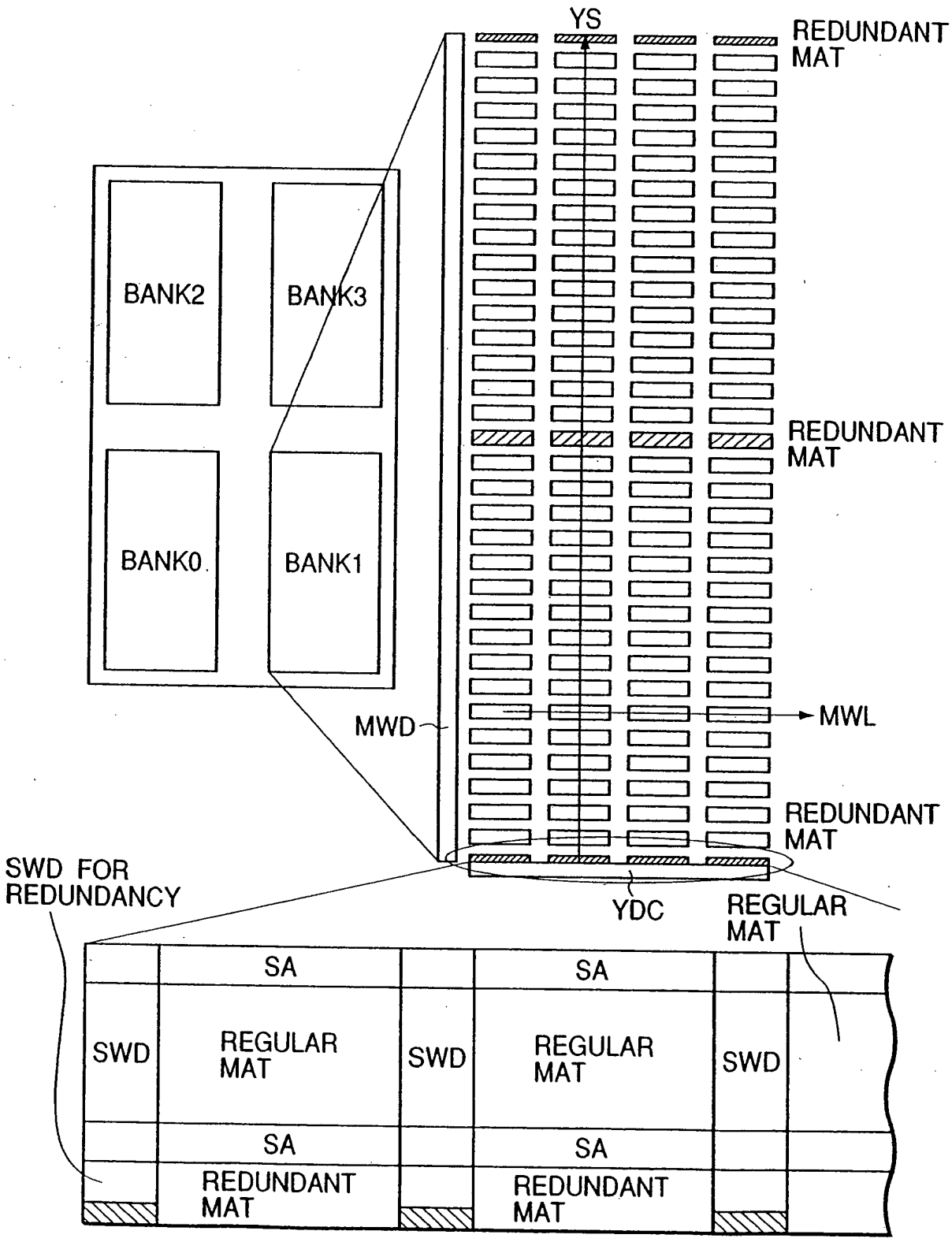

YS
REDUNDANT MAT
BANK2
BANK3
BANK0
BANK1
REDUNDANT MAT
MWD
MWL
REDUNDANT MAT
SWD FOR REDUNDANCY
YDC
REGULAR MAT
SA
SA
SWD
REGULAR MAT
SWD
REGULAR MAT
SWD
SA
SA
REDUNDANT MAT
REDUNDANT MAT

FIG. 21

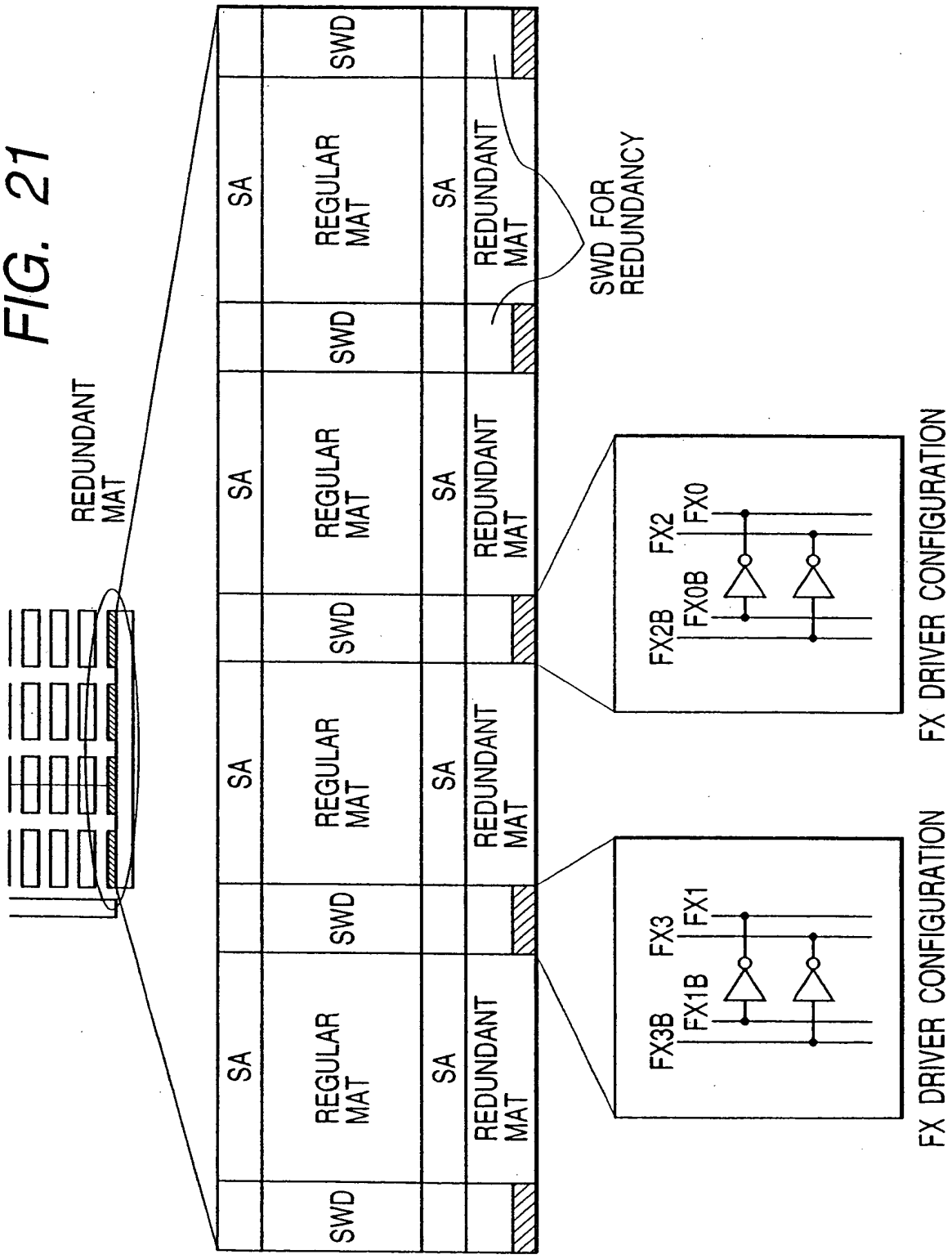

REDUNDANT MAT
SWD
SA
REGULAR MAT
SWD
SA
REGULAR MAT
SWD
SA
REGULAR MAT
SWD
SA
REDUNDANT MAT
SWD FOR REDUNDANCY
FX3B
FX3
FX1B
FX1
FX2B
FX2
FX0B
FX0
FX DRIVER CONFIGURATION
FX DRIVER CONFIGURATION

FIG. 22

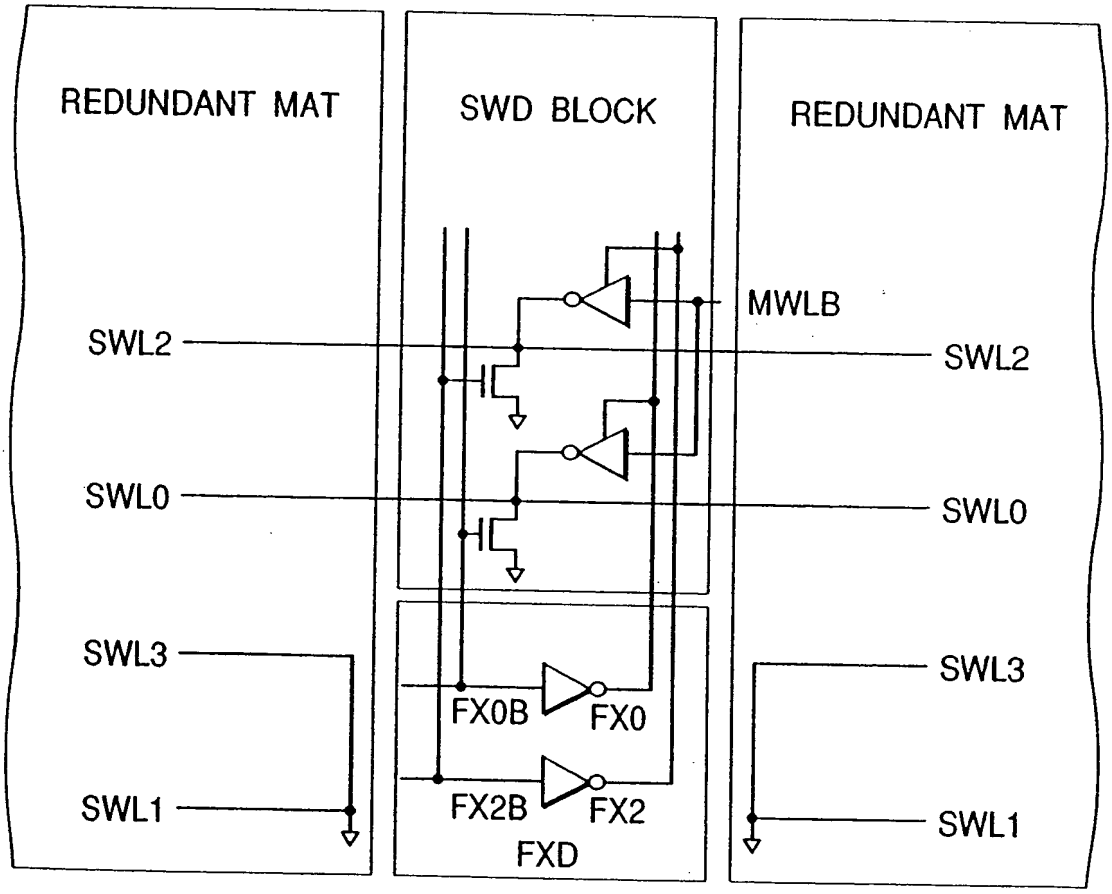

REDUNDANT MAT
SWD BLOCK
REDUNDANT MAT
MWLB
SWL2
SWL2
SWL0
SWL0
SWL3
SWL3
FX0B
FX0
SWL1
FX2B
FX2
SWL1
FXD

FIG. 23

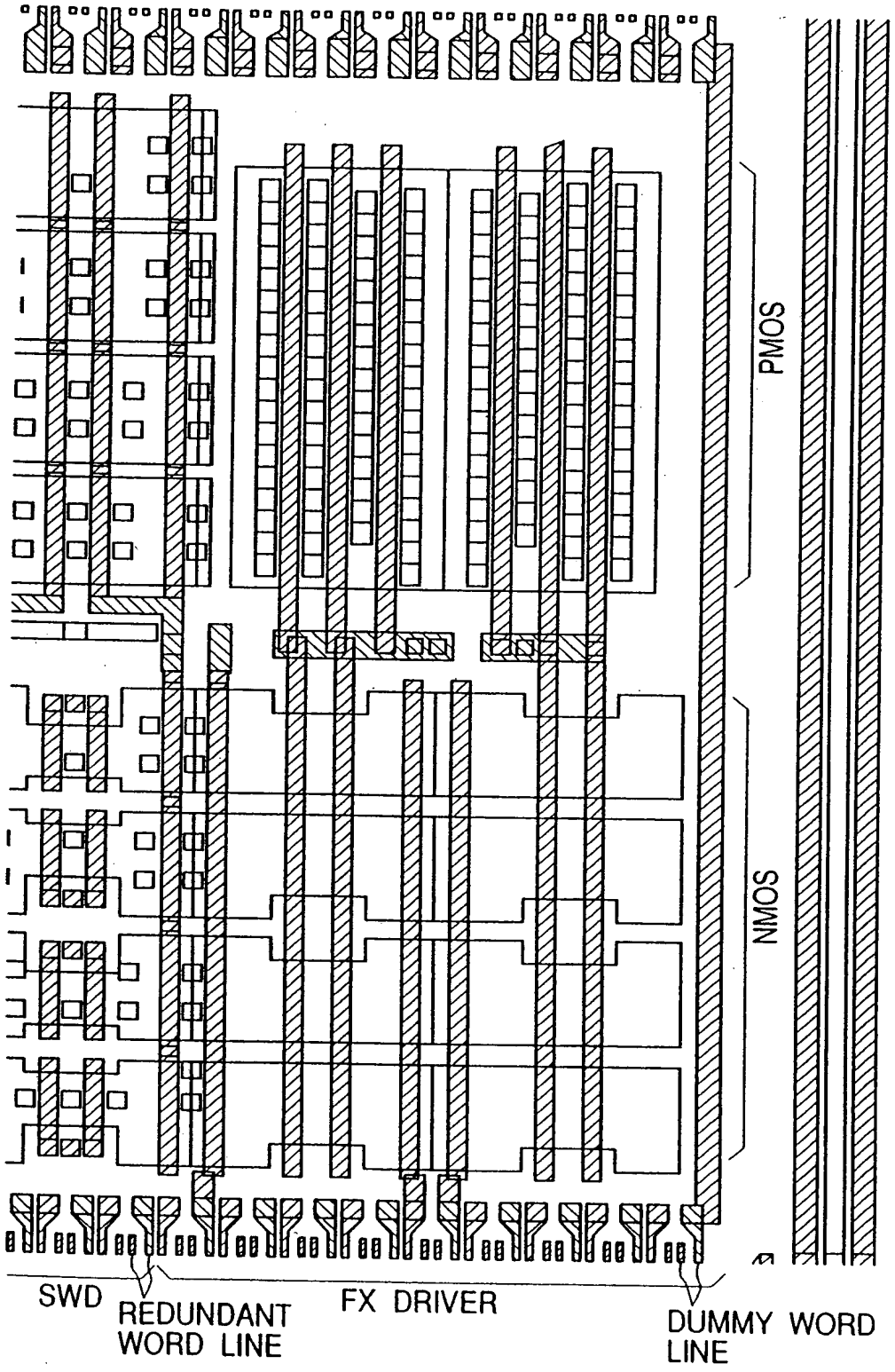


FIG. 24

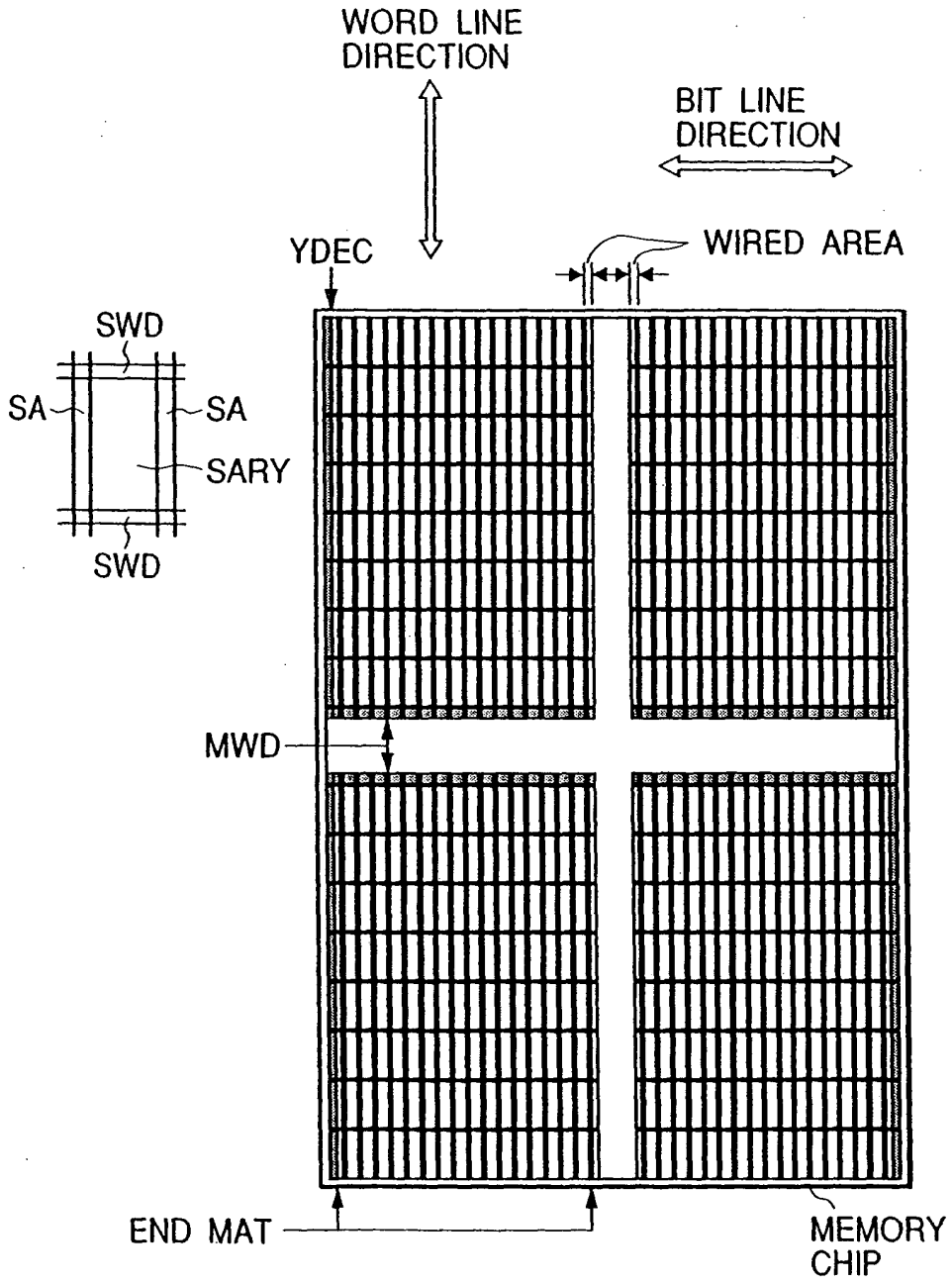
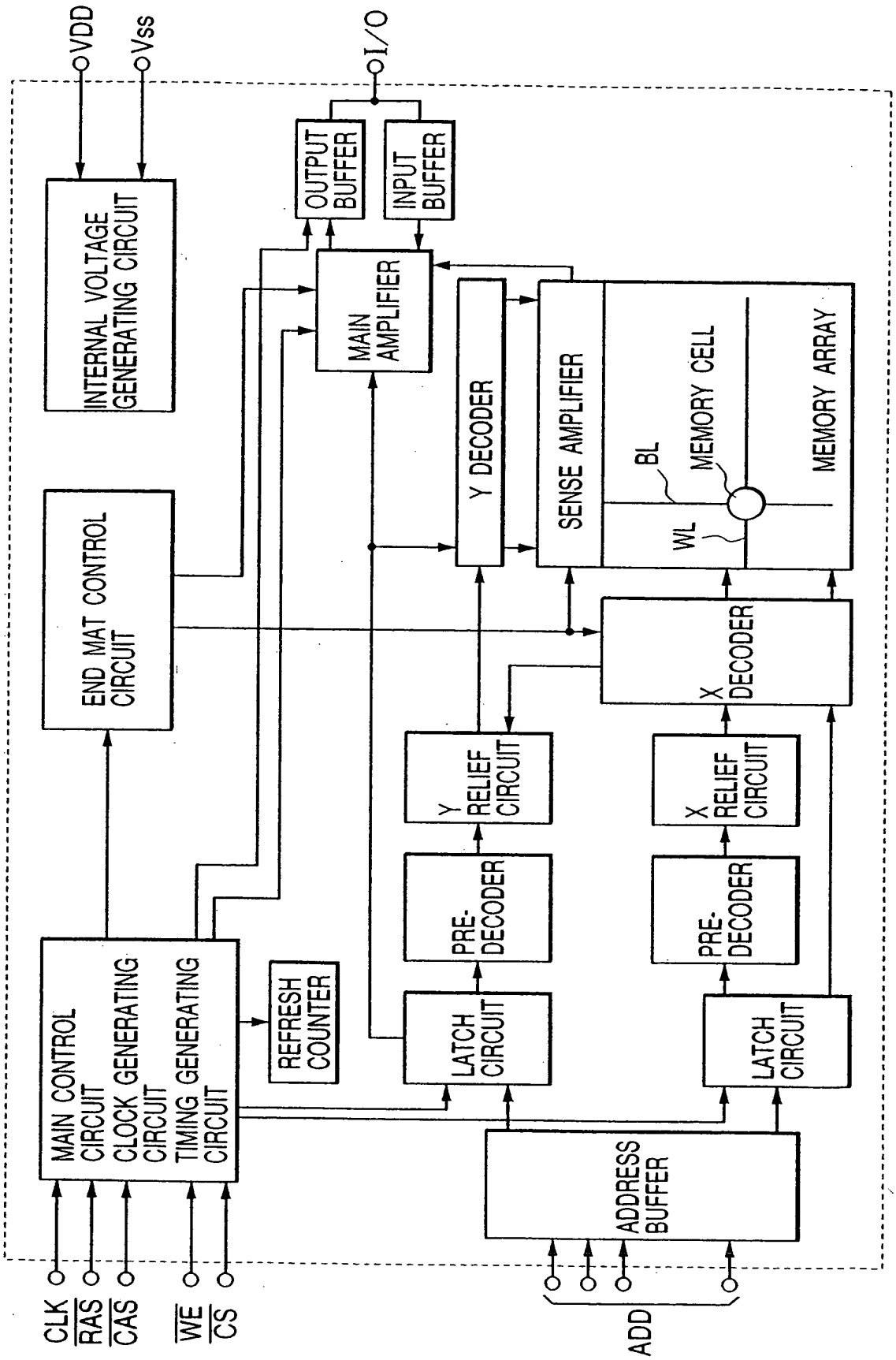

WORD LINE DIRECTION
BIT LINE DIRECTION
YDEC
WIRED AREA
SWD
SA
SA
SARY
SWD
MWD
END MAT
MEMORY CHIP

FIG. 25


VDD
Vss
I/O
INTERNAL VOLTAGE GENERATING CIRCUIT
OUTPUT BUFFER
INPUT BUFFER
MAIN AMPLIFIER
Y DECODER
SENSE AMPLIFIER
BL
MEMORY CELL
WL
MEMORY ARRAY
END MAT CONTROL CIRCUIT
X DECODER
Y RELIEF CIRCUIT
X RELIEF CIRCUIT
PRE-DECODER
PRE-DECODER
MAIN CONTROL CIRCUIT
CLOCK GENERATING CIRCUIT
TIMING GENERATING CIRCUIT
REFRESH COUNTER
LATCH CIRCUIT
LATCH CIRCUIT
ADDRESS BUFFER
CLK
RAS
CAS
WE
CS
ADD